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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,396	06/07/2001	Syuuichi Kariyazaki	14701	7345

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EXAMINER	
COSTANZO, PATRICIA M	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/876,396	Applicant(s) KARIYAZAKI, SYUUICHI	
	Examiner Patricia M. Costanzo	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification contains terms that are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact, or verbose terms used in the specification are:

a. page 11, lines 17 – 20: the use of the antecedent "a" to denote "dielectric substrate" makes unclear on which dielectric substrate "a specified interconnect pattern is formed;"

b. page 12, line 5: in referring to Figure 5, the text refers to ball electrodes (31), however there is no reference number (31) in Figure 5;

c. page 14, line 19: is "21b" supposed to be "22b"?

d. page 16, lines 3 and 4: the terms endlessly and annually are ambiguous and should be replaced by more definitive terms; and

e. page 17, lines 24 and 25: the acronyms GND and VDD should be defined after their first occurrence in the text.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites, in part, " . . .wherein the mounting member is a semiconductor package mounting a semiconductor chip on a package substrate. .. and the substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon."

Terms such as "the mounting member", "a semiconductor package", "a package substrate", "the substrate", and "a mounting substrate" present problems. For one, the repeated use of the term substrate, albeit with different words confuses what is meant when substrate is used. In addition, there could be an antecedent problem, but whether there is an antecedent problem is impossible to ascertain without a clear definition of the terms used in the claim.

In Claim 1, the semiconductor chip is mounted on the mounting member. In Claim 3 the mounting member is defined as a semiconductor package and the semiconductor is mounted on a packaging substrate, but at the end of the claim "the substrate is a mounting substrate for . . . mounting the semiconductor package thereon." The semiconductor package however contains the semiconductor substrate.

Clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 - 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent Application Publication, Application No. 09/203,196 (Yoon *et al.*) (see Figures 1A – 6C and respective portions of the Yoon *et al.* specification), in view of United States Patent No. 6,285,560 (Lyne) (see Figures 1 – 14 and respective portions of the Lyne specification) and United States Patent No. 6,310,398 (Katz) (see Figures 1 – 26 and respective portions of the Katz specification).

Referring to Claim 1: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device (see, for example, [0019]) comprising:

a semiconductor member (see, for example, [0049] and [0050] and Claim 13) having thereon a plurality of interconnect pads (see, for example, [0050]): and

a mounting member (see, for example, Figure 2 (20)),

the electrode terminals (see, for example Figure 4 and Figure5A (25)) forming a plurality of I/O cells (see, for example [0036]) each having part of the electrode terminals, the part of electrode terminals including signal terminals, the I/O cells forming a first group of the I/O cells and a second group of I/O cells disposed on an inner position of the mounting member with respect to the first group (for example, see such a pattern illustrated in Figure 5A).

Note: The technique of "depopulating" peripheral electrodes to produce a gap between peripheral electrodes through which additional routing traces or lines can be extended to provide for additional electrodes in the inner space bordered by the peripheral electrodes, is well known. See Lyne, Figure 8, and Katz, Figure 16 for support.

Yoon *et al.* do not explicitly disclose that the mounting member includes having a plurality of electrode terminals electrically and mechanically connected to the respective interconnect pads for mounting the semiconductor chip on the mounting member, although they do disclose that wire bond pads (Figure 5A (24)) are formed such that the package body (Figure 2 (20)) is connected (not illustrated but see, for example, [0050]) the semiconductor chip by a wore bonding or other connecting methods such as redistribution for wager level

packaging method and C4 (controlled Collapsed Chip Connection) method. To have the package body electrically attached to a chip would necessitate the presence having a plurality of electrode terminals electrically and mechanically connected to the respective interconnect pads.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the packaging substrate disclosed by Yoon *et al.* by providing for a mounting member having plurality of electrode terminals electrically and mechanically connected to the respective interconnect pads for mounting the semiconductor chip on the mounting members to obtain the advantage of having electrical and mechanical functioning connections to provide for a functioning electrical device.

Referring to Claim 2: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the semiconductor member is a semiconductor chip (see, for example, first two sentences of [0037], the electrode terminals are internal electrodes disposed on a bottom surface of the semiconductor chip (it is inherent that there are connecting electrode terminals on the connecting surface of the chip for reasons given above, see discussion relating to Claim 1 and pads on chip) and the mounting member is a package substrate ((20) Figure 2) used for packaging thereon the semiconductor chip.(see, for example, [0037]).

Referring to Claim 3: In as much as Claims I and 3 are in compliance with 35 U.S.C. 112, and as well as indefinite claims can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the mounting member is a semiconductor package (see, for example, the package (20) as illustrated in Figure 2) mounting a semiconductor chip (not shown, but disclosed in text, see, for example, [0019]) on a packaging substrate (see, for example, [0054]), the electrode terminals are ball electrodes (see, for example, third sentence of [0050]) disposed on a bottom surface of the packaging substrate, and the substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon (see, for example, Figures 4 and 5A and/or [0054]).

Referring to Claim 4: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the I/O cell (see, for example, third sentence of [0037]) includes only the electrode terminals (see, for example, Figure 4) for signals (see, for example, [0057]) or the electrode terminals for signals and power (see, for example, third sentence of [0037], intermingled among one another.

Yoon *et al.* do not explicitly discuss the presence of a ground electrode terminal. Without a ground, however, the device would not work, and thus the presence of a ground terminal is inherent in a working device.

Referring to Claim 5: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the I/O cell includes peripherals (see, for example, peripherals as illustrated in Figure 5A).

Referring to Claim 6: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein an interconnect line is connected to the interconnect pad, and the interconnect lines connected to the interconnect pad of the at least one of the I/O cells are formed in a single interconnect layer (see, for example, interconnect lines and pads formed in a single layer illustrated in Figure 5A).

Referring to Claim 7: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the substrate includes the interconnect pad and the interconnect line electrically connected to the interconnect pad in the single interconnect layer formed on the surface of the substrate (see, for example, Figure 5A and [0046].

Referring to Claim 8: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the interconnect lines connected to the I/O cells located on inner positions extend

between the I/O cells located on the outer periphery (see, for example, Figure 5A)

Note: As mentioned above, the technique of "depopulating" peripheral electrodes to produce a gap between peripheral electrodes through which gap additional routing traces or lines can be extended to provide for additional electrodes in the inner space bordered by the peripheral electrodes, is well known. See Lyne, Figure 8, for example, and Katz, Figure 16, for example, for support.

Referring to Claim 9: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate (see, for example, Figure 2 and Figure 4).

Referring to Claim 10: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein at lease one of the first group and the second group includes an outer group and an inner group disposed on the inner position of the mounting member with respect to the outer group (see, for example, Figure 5A. See also, Lyne, Figure 8, and Katz, Figure 16, for additional examples of this well-known technique.

Referring to Claim 11: In as much as Claim I is in compliance with 35 U.S.C. 112, and as well as an indefinite claim can be understood, Yoon *et al.* disclose a semiconductor device as recited above, further disclosing wherein the interconnect lines connected to the interconnect pads corresponding to the first I/O cells and the interconnect lines connected to the interconnect pads corresponding to the second I/O cells are formed in different interconnect layers (see, for example, Figure 4 (20-1), (20-2), (T), and (22)).

Conclusion

Any inquiry concerning this communication should be directed to Patricia Costanzo at 703 305-5675 on Monday – Friday from 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful Supervisory Primary Examiner Tom Thomas can be reached at 703 308 -2772.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist at 703 308-095.

Tom Thomas

pmc
March 20, 2002

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